2023 International RF-SOI Workshop

Pudong Shangri-La, Shanghai

2023.10.24

Addressing the Challenges for RF Front-end Module Designs

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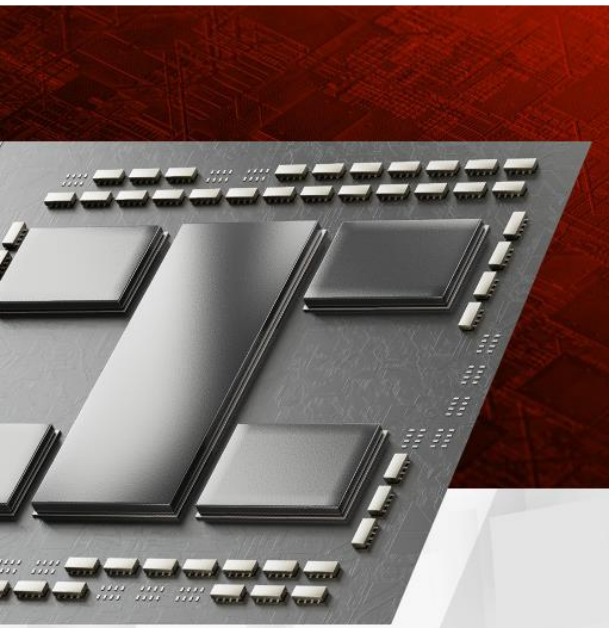
Founder & CEO, Xpeedic

Oct 24, 2023

XPEEDIC

ACCELERATE YOUR IC DESIGN

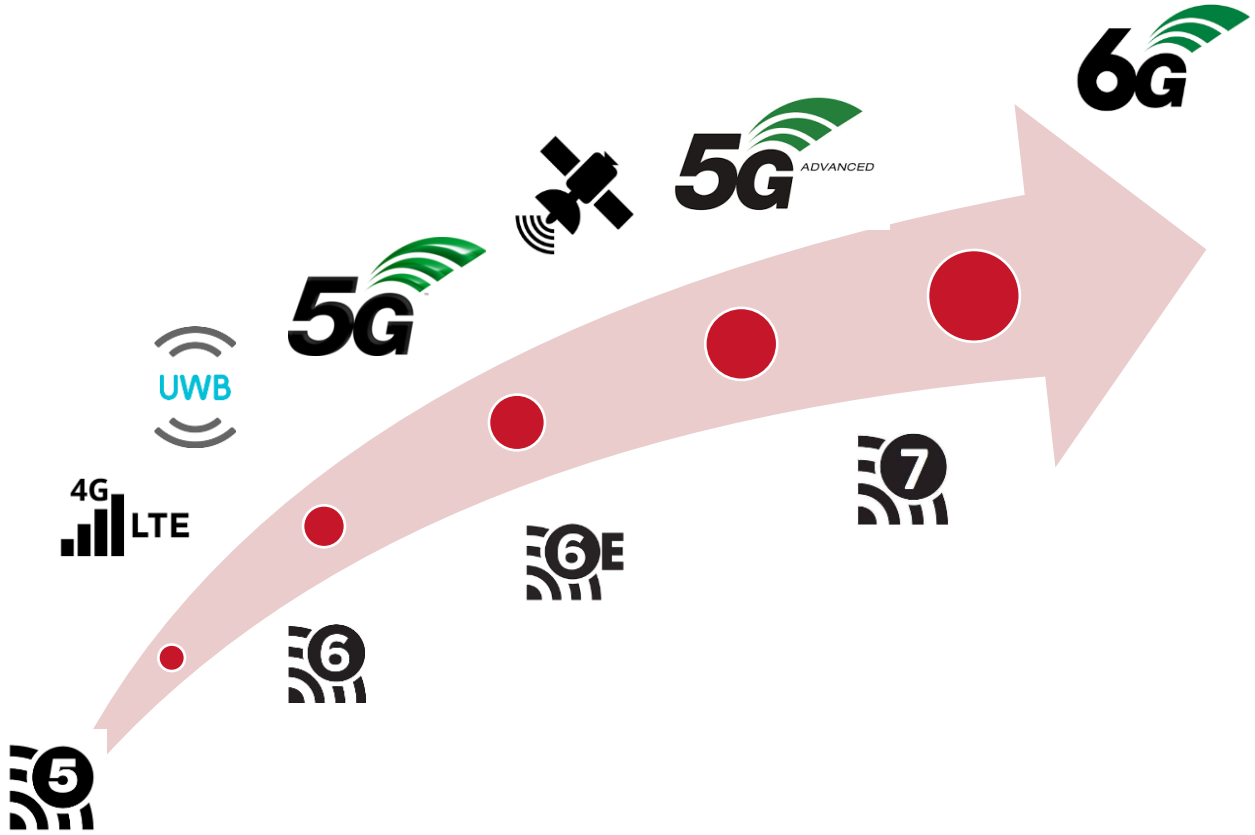
CONTENT



1

RFFE Market Trend and Design Challenges

Megatrend: Wireless Technology Evolution



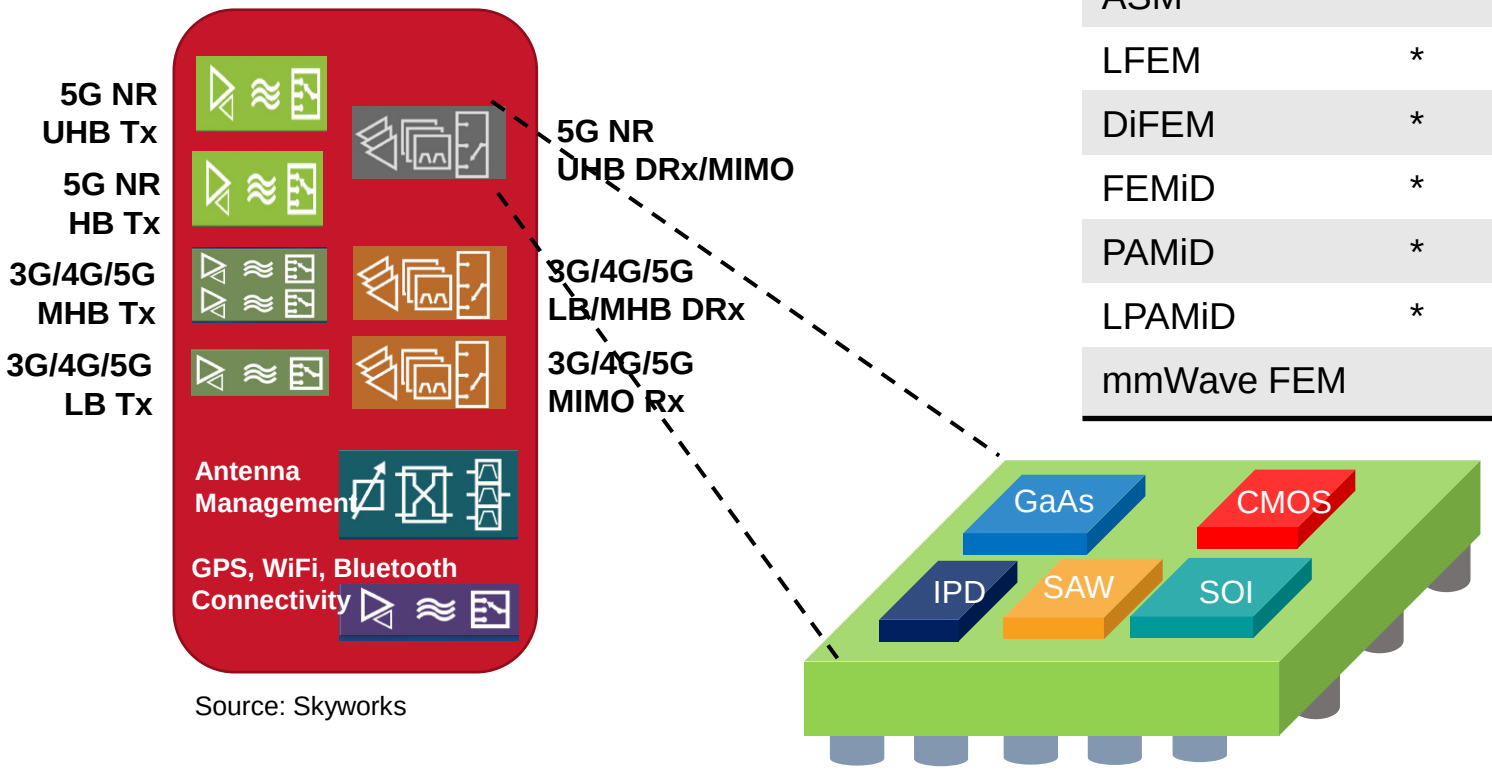
- Capacity and data rate
  - Sub-6GHz, mmwave
  - More CA combinations
  - Dual connectivity (EN-DC, NR-DC)
- More services
  - GNSS (L2,L5)
  - Satellite support

System Complexity Drives RFFE Component Technology

- System complexity adds additional requirements for components, which determines the choice of process technology

Component	Requirement	Process
PA	• Multi channel • Multi band • +3 dB linear	GaAs HBT GaAs Bi-HEMT
LNA	• DL MIMO • Multi channel • Multi band • Switch integration	RF SOI SiGe BiCMOS CMOS
Switch	• CA/MIMO • More pole/throw	RF SOI CMOS
Tuner	• Wide range • Efficiency • Linearity	RF SOI/CMOS MEMS
Filter	• Multi band • Steep rejection • High sensitivity/Low IL	SAW,TC-SAW, TF-SAW BAW,FBAR,XBAR MLCC,IPD

System Complexity Drives RFFE Modularization

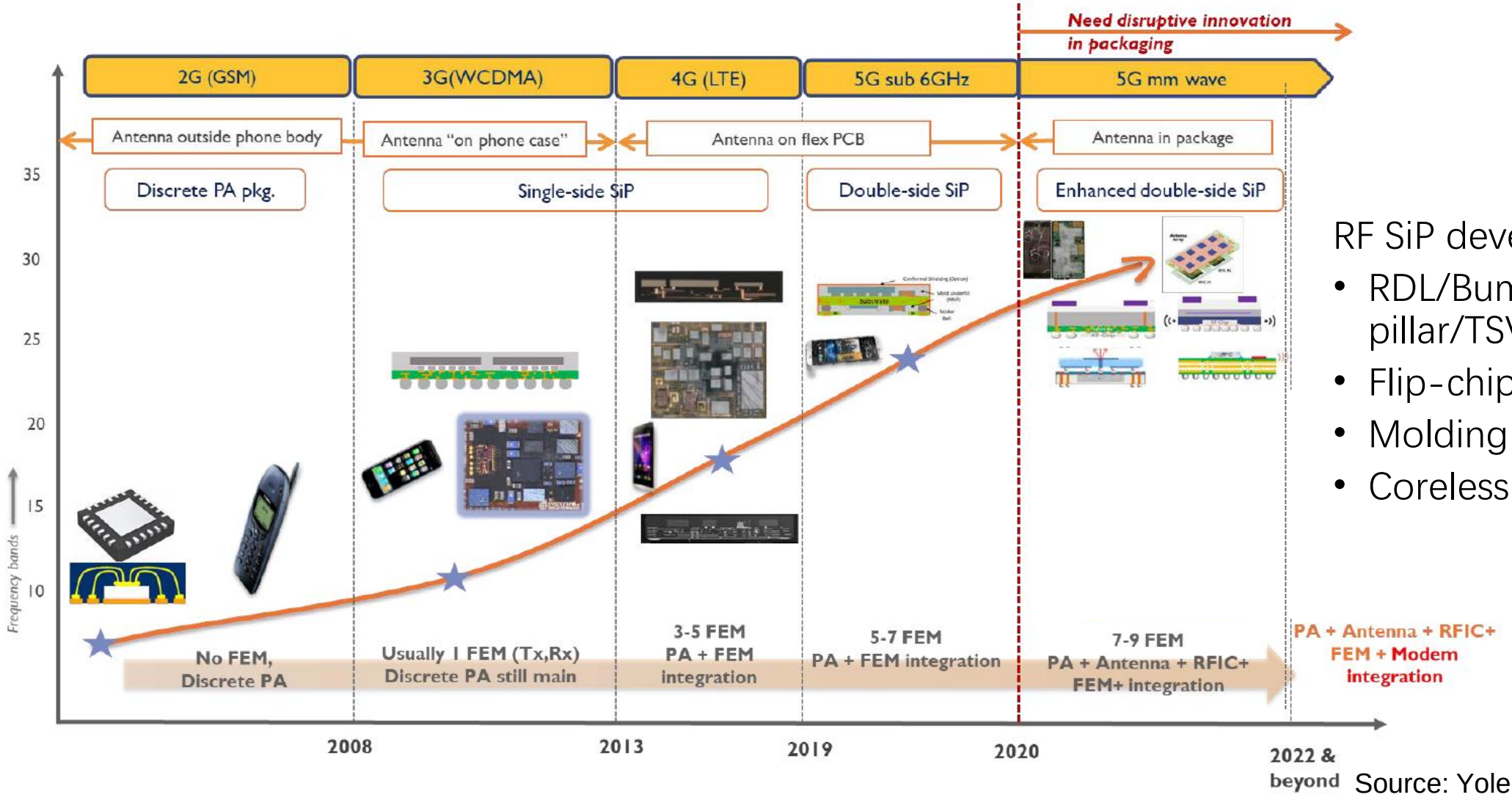


Source: Skyworks

	Filter	PA	LNA	Switch	Duplexer	Antenna
ASM	*			*		
LFEM	*		*	*		
DiFEM	*			*		
FEMiD	*			*	*	
PAMiD	*	*		*	*	
LPAMiD	*	*	*	*	*	
mmWave FEM		*			*	*

- System-in-Package (SiP) enables the integration of PA, LNA, switch, and filter, which are typically manufactured with different process technologies, into one module.

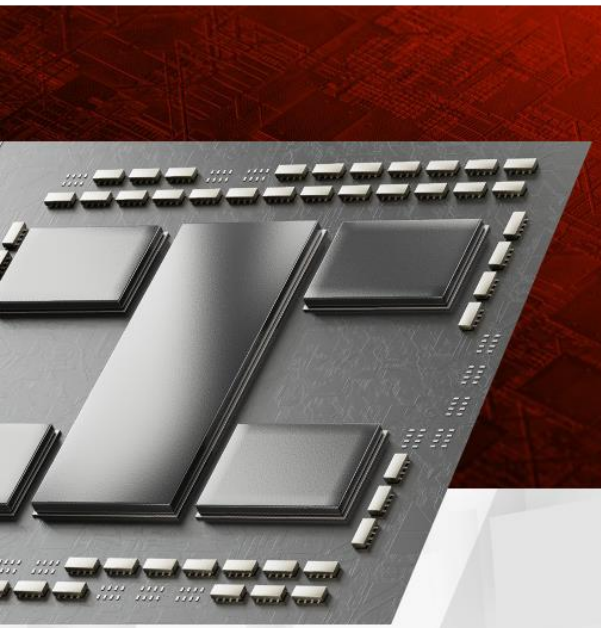
RF SiP Enables RFFE modularization



RF SiP development

- RDL/Bumbing/Cu pillar/TSV
- Flip-chip/Wire-bond
- Molding
- Coreless substrate

Source: Yole



2

RFFE Design: EDA Perspective

RF Front-end Module Design Challenges

RF System level optimization

Component level insufficient

Co-simulation and co-design

Component-to-component co-simulation

Die and package co-simulation

Multiphysics analysis

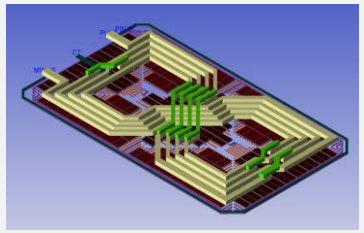
Thermal and stress simulation

Unified EDA environment

Seamless integration of different tools

Xpeedic Simulation Toolset for RFFE Designs

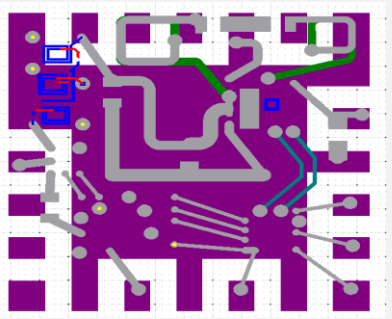
RFIC



IRIS

- IRIS: on-chip EM simulation tool
- Qualified on various process technologies including RFSOI, GaAs,and SiGe BiCMOS.

RF Module



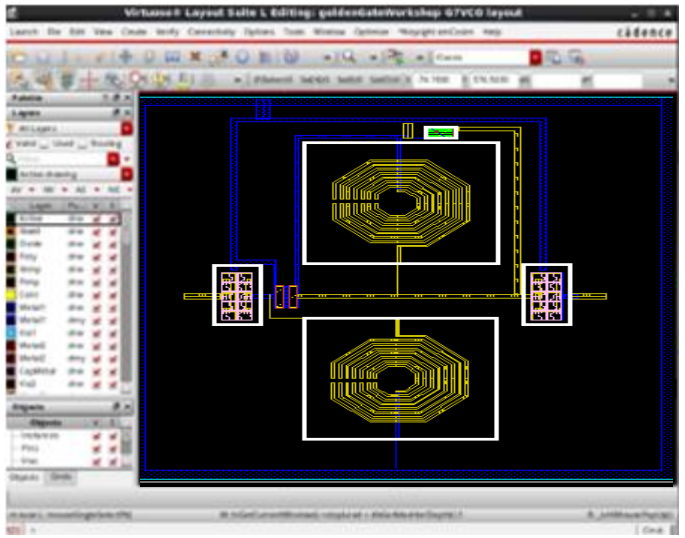
HERMES

- HERMES: 3D RF module EM simulation tool
- Support various WB/FC packages
- Support IC-package co-simulation
- Support lumped and wave ports

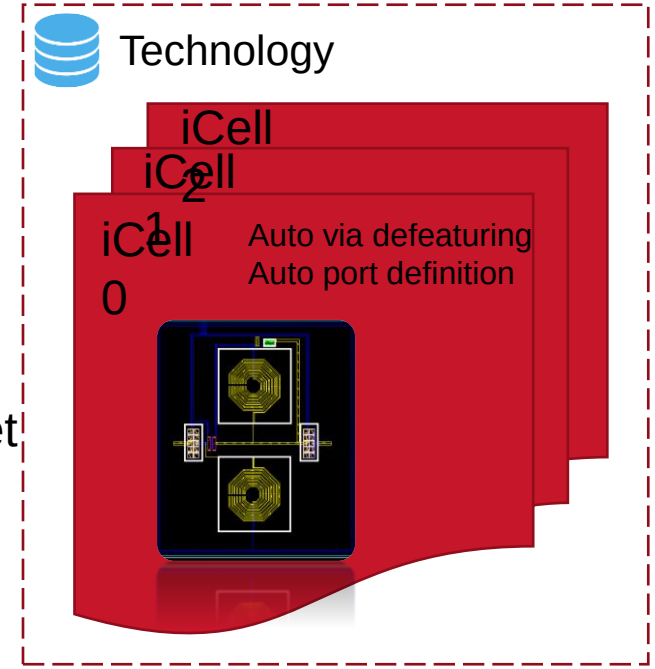
XDS

- XDS: RF system level design and simulation platform
- Schematic circuit-level design and optimization
- EM-circuit co-simulation

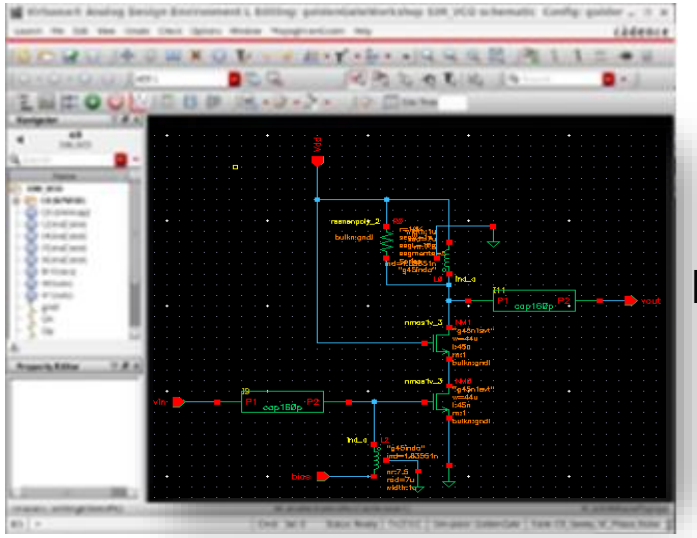
IRIS: On-chip EM Simulation Tool



Select
Instance/net



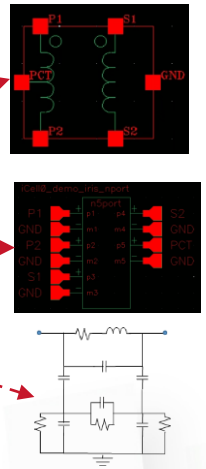
- Mixed rect-tri mesh
- Fast MoM solver
- LSF, PBS, SGE



Back-annotate

- auCdl
- auLvs
- Symbol
- Schematic_nport
- Schematic_ckt
- Schematic_pz

Multiple views



IRIS Support Mainstream IC Processes

Bulk | FinFET | FD-SOI | RF-SOI | SiGe BiCMOS | GaAs | RF

- TSMC: 40nm, 28nm, 22nm
- UMC: 28nm, 40nm
- SMIC: 55nm, 40nm, 28nm
- CSMC
- GLOBALFOUNDRIES: 12LP
- SAMSUNG SEMICONDUCTORS: 14LPP, 8LPP
- SMIC: 14nm
- GLOBALFOUNDRIES: 22FDX
- SAMSUNG SEMICONDUCTORS: 28FDS
- GLOBALFOUNDRIES: 8SW
- TPSCo: TPS9
- xfab: XR013
- ST: H9SOI
- GLOBALFOUNDRIES: 8HP, 9HP
- TOWERJAZZ: SBC18
- ST: B55
- win SEMICONDUCTORS
- A
- SMIC
- TSMC
- ST
- ON Semiconductor

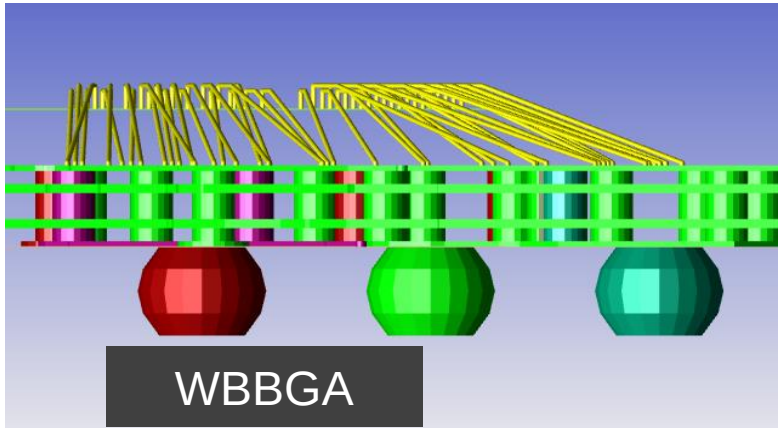
HR Silicon

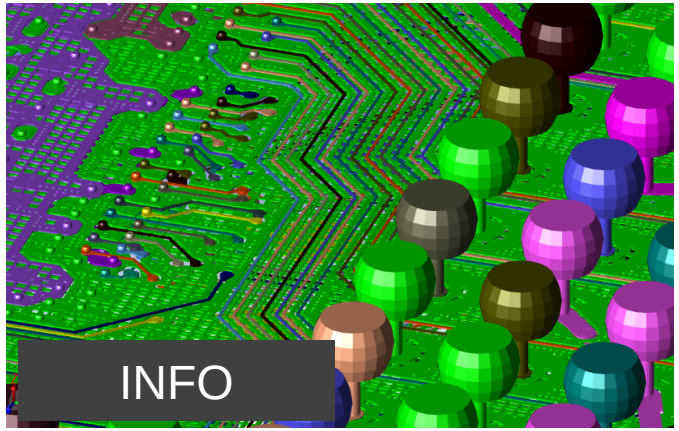
CORNING

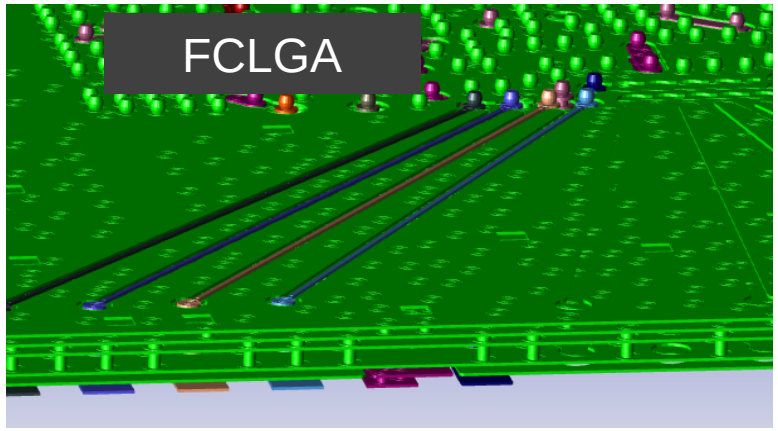
TGV

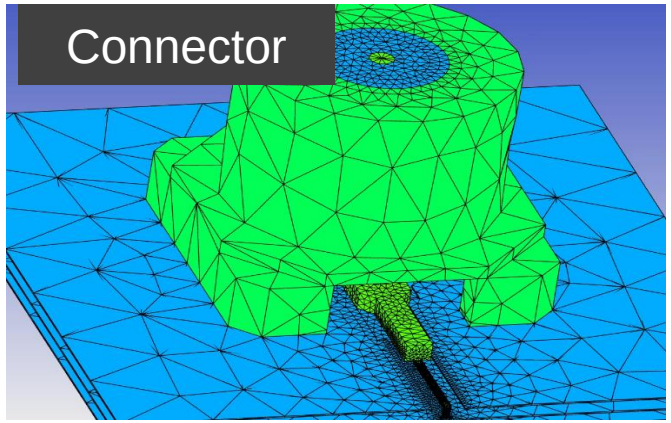
HERMES: 3D EM Simulator for RF Module

- Support arbitrary 3D structures with solve frequency up to THz
- Support multiple port types: wave port, regular lumped port, irregular lumped port, coaxial port





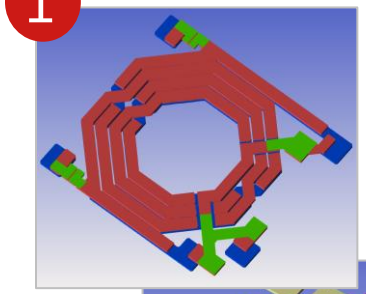




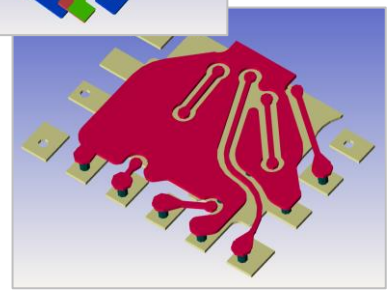
HERMES: support IC/package assembly

1

DIE



PKG



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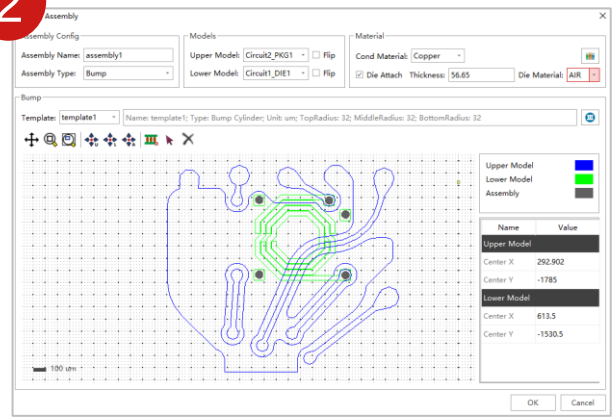
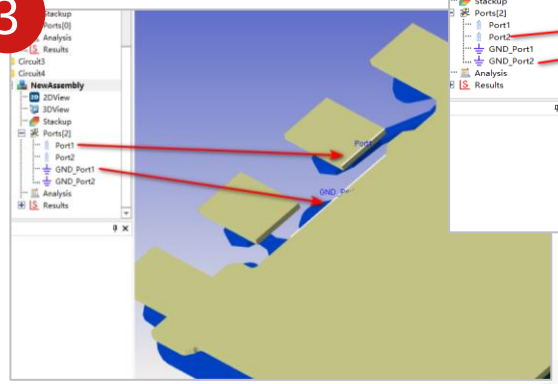
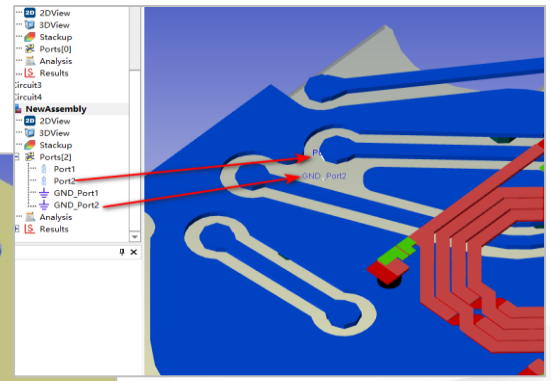


Assembly

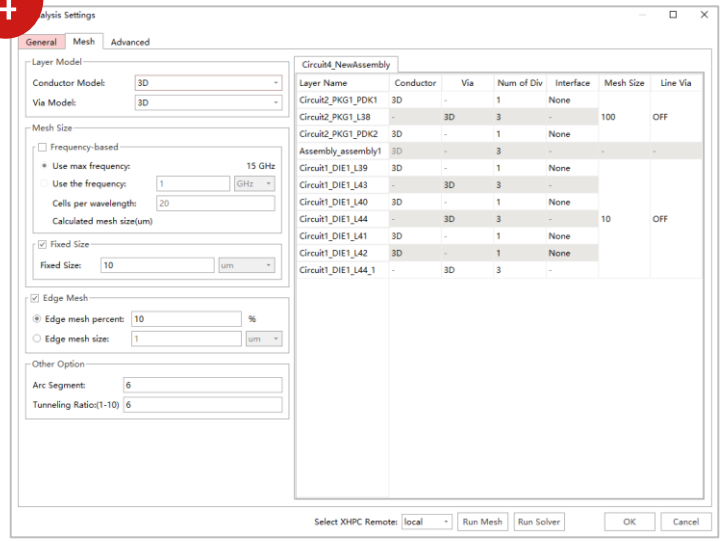
3





4

Solver setting



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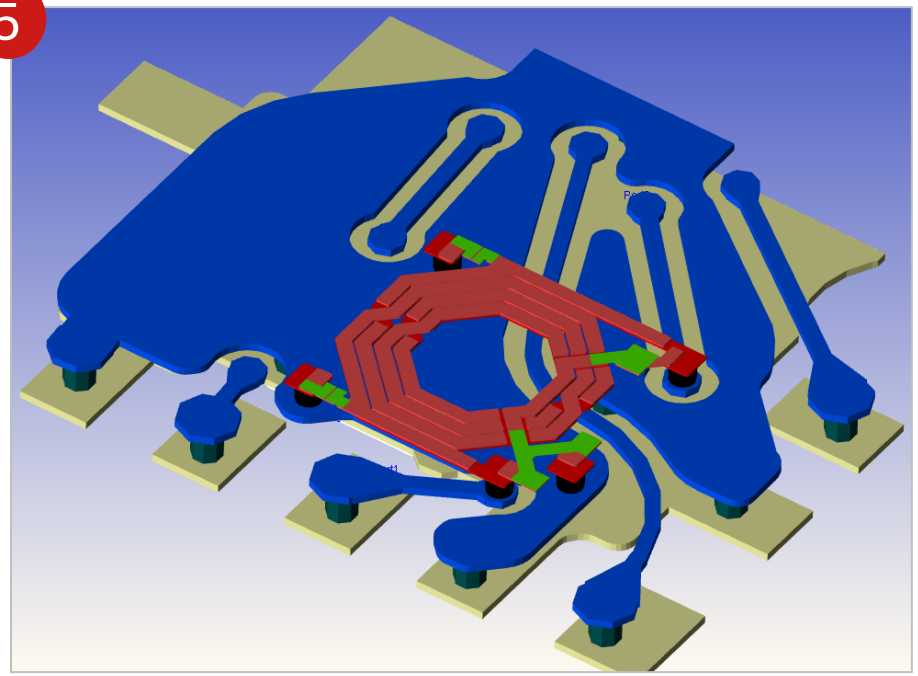
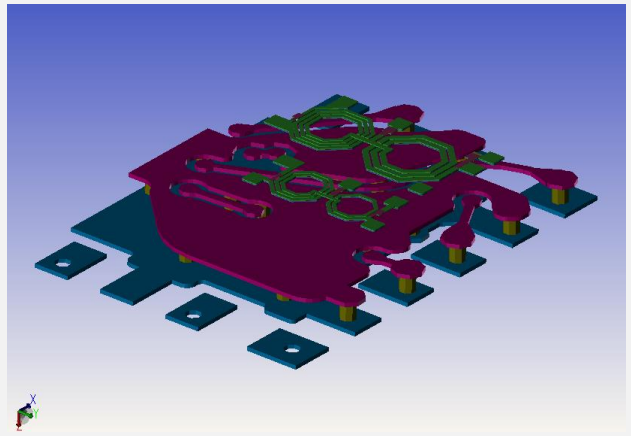
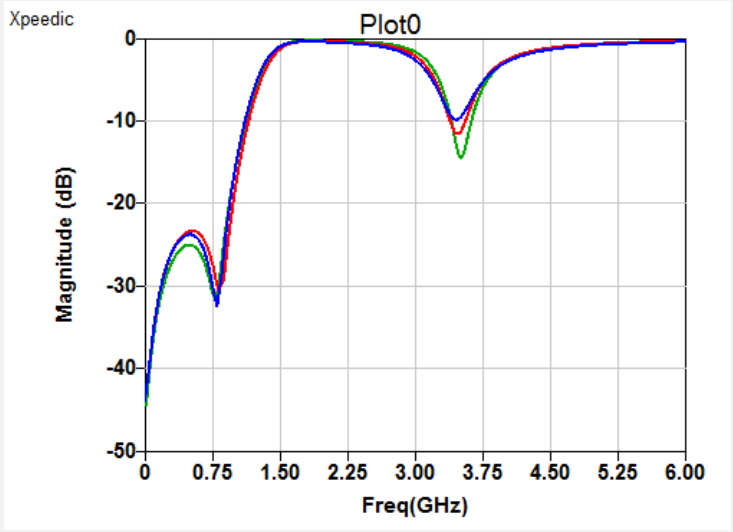
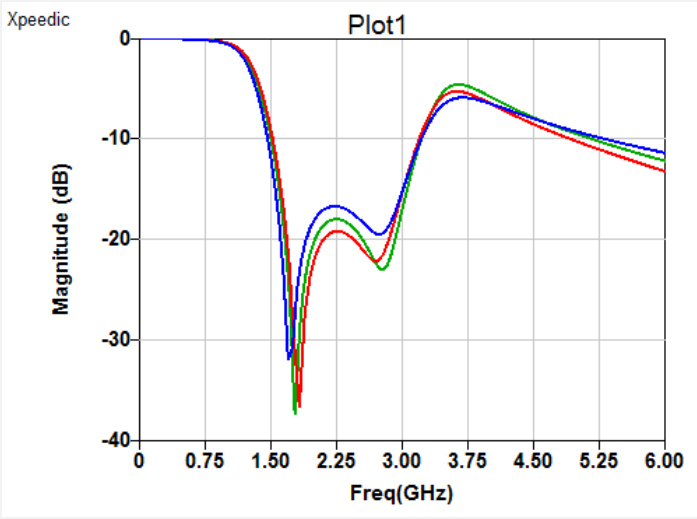


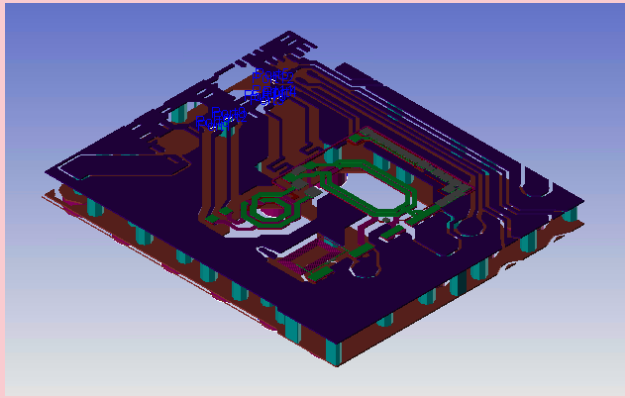
HERMES for RFFE Module Examples



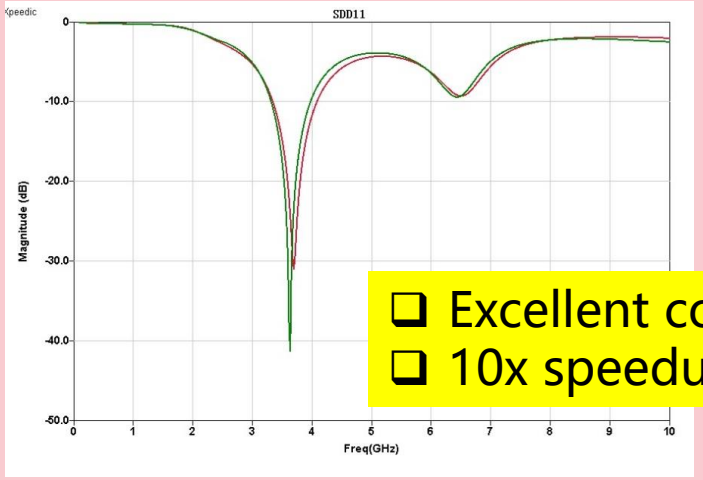
RFFEM in QFN package

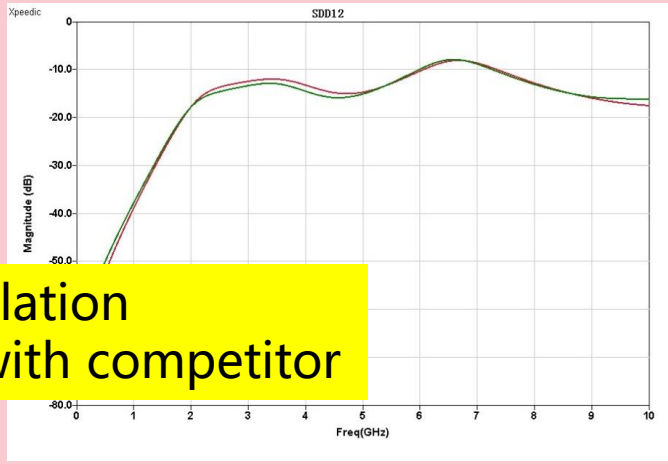






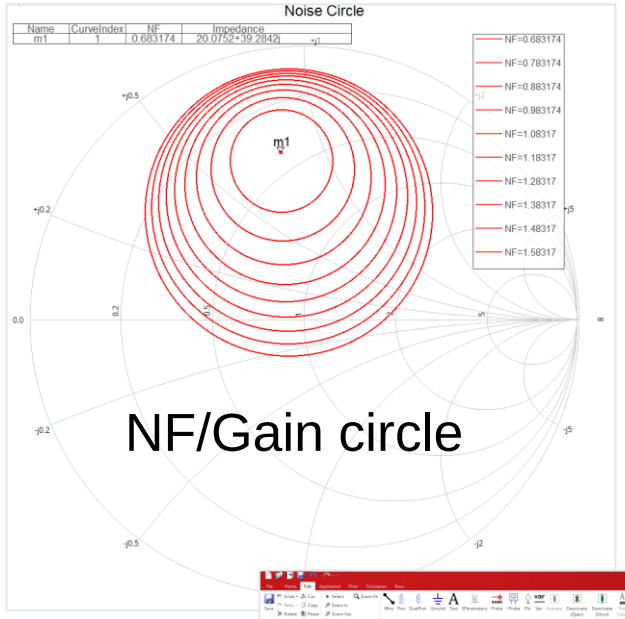
RFFEM in BGA package



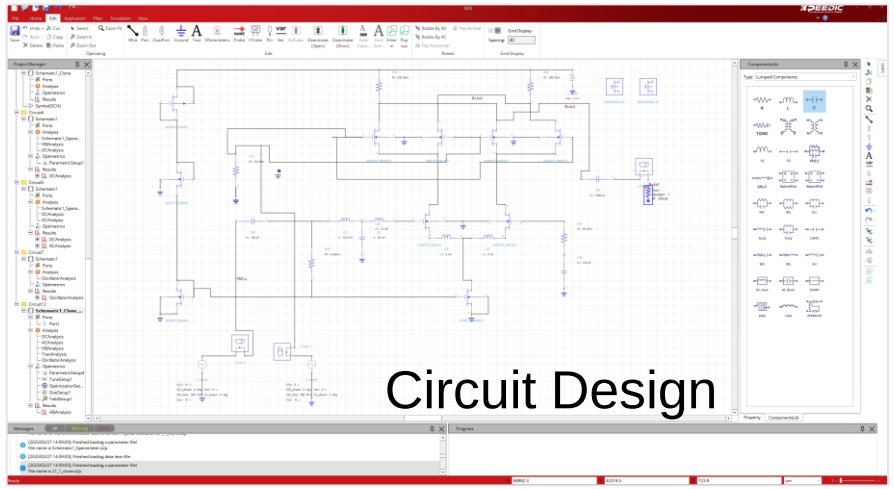


- ❑ Excellent correlation
- ❑ 10x speedup with competitor

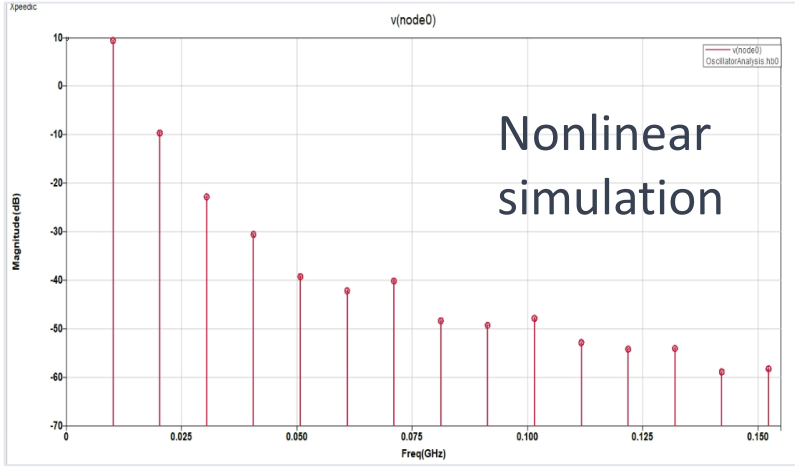
XDS: Design and Analysis of RF IC Circuits



NF/Gain circle

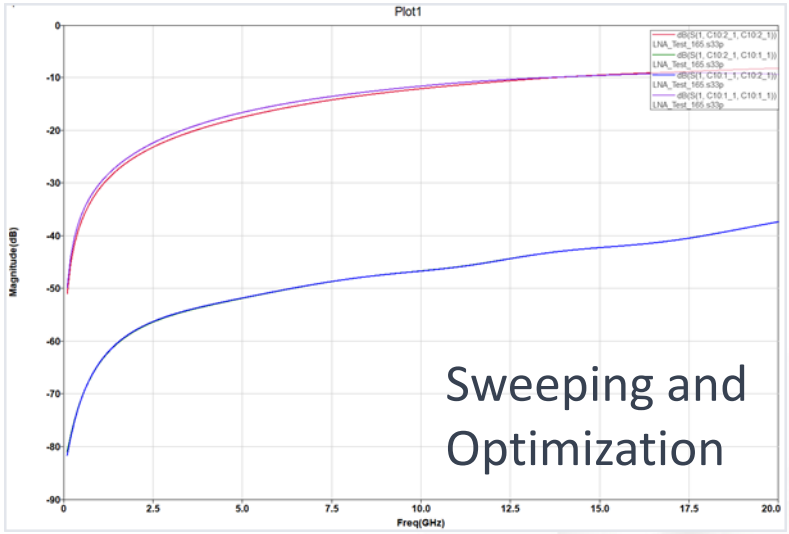


Circuit Design



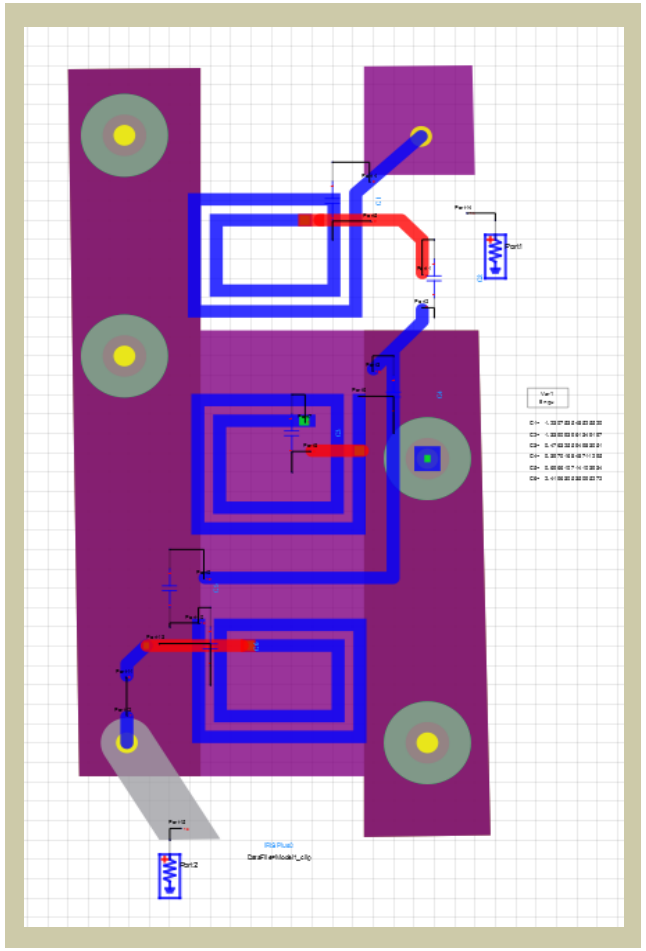
Nonlinear simulation

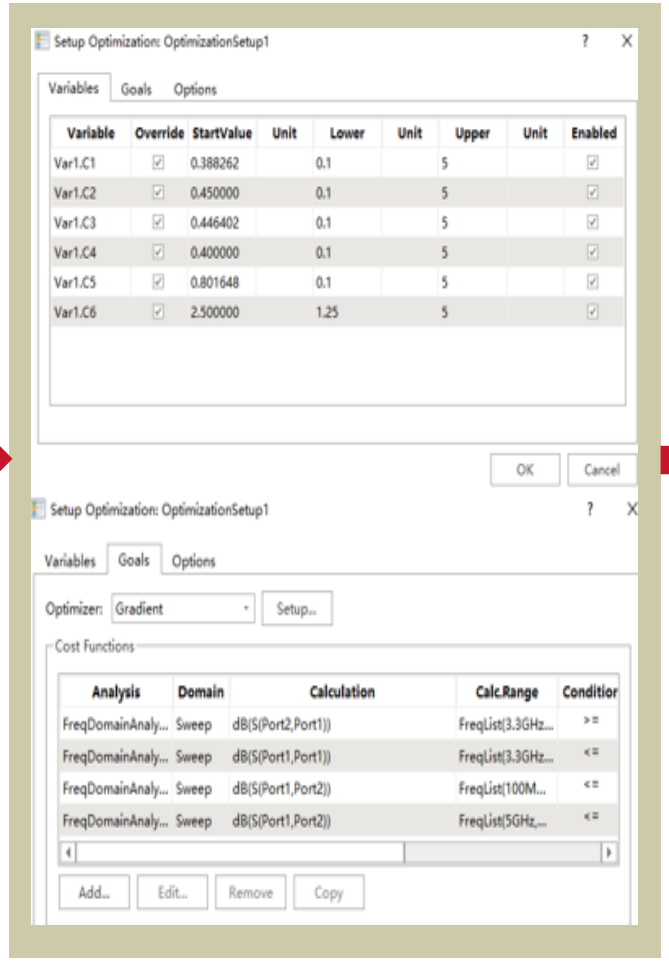
Time Domain



Sweeping and Optimization

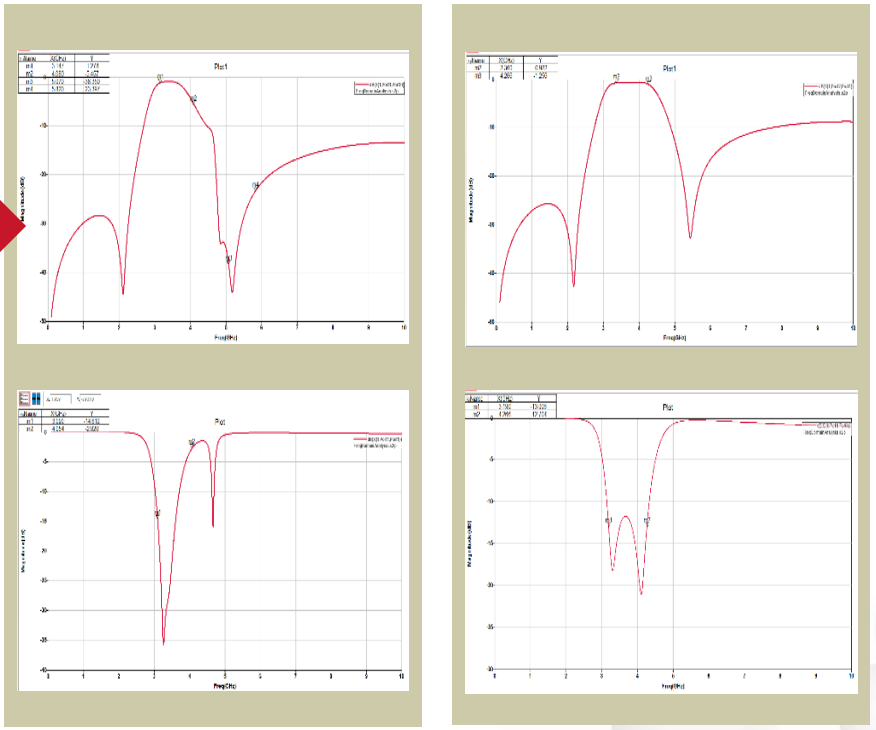
XDS Support Circuit Optimization





original

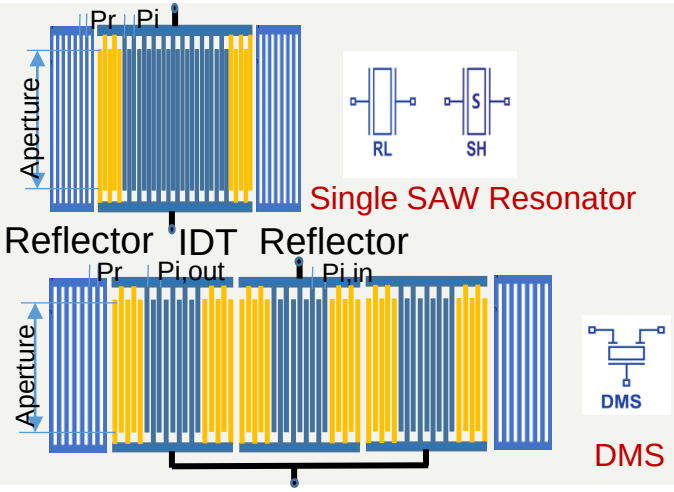
optimized

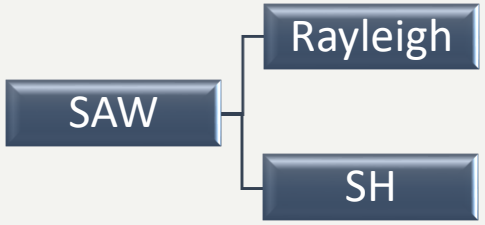


Optimization option

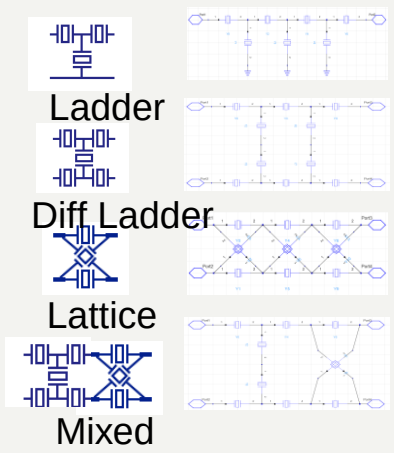
XDS Support SAW/BAW Design

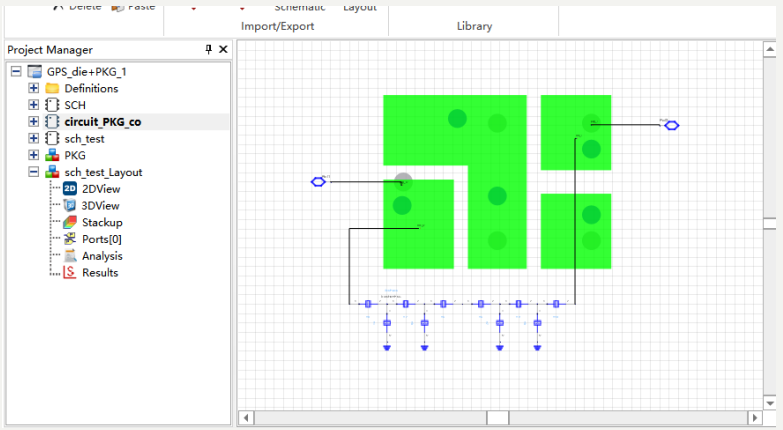
- SAW device
  - Single SAW resonator
  - Double Mode SAW (DMS)
- BAW mBVD / Mason model
- Waves types
  - Rayleigh waves
  - SH waves

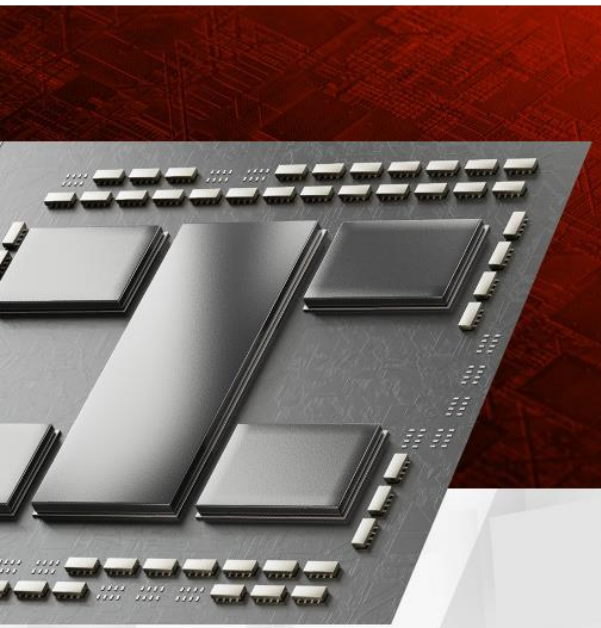




- Topology
  - Ladder
  - Lattice
  - Mixed ladder-lattice
- device and package co-sim



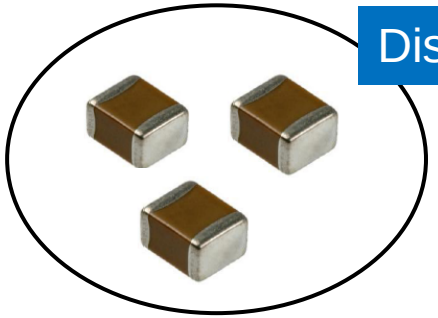




3 IPD for RFFE Module

IPD for RFFE Integration and Miniaturization

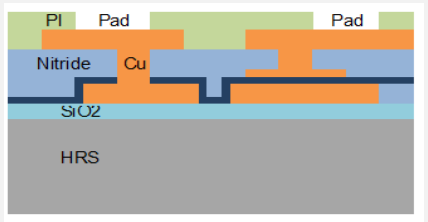
- Integrated Passive Device (IPD) advantages over discrete



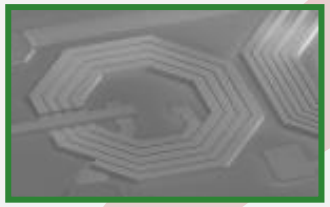
- Discrete R, L,C
- Bulky
- Poor tolerance control

- Multiple R, L, C
- Small size, low profile
- High performance
- Consistency
- High integration

IPD Evolution for RF Front-end



High Resistivity Silicon (HRSi)



IPD 1.0

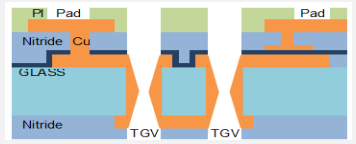
- HRSi

IPD1.5

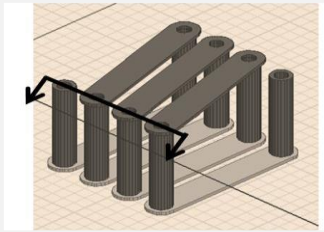
- HRSi+RDL

IPD 2.0

- TGV



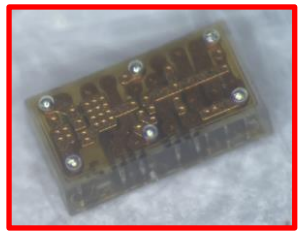
Through Glass Via (TGV)



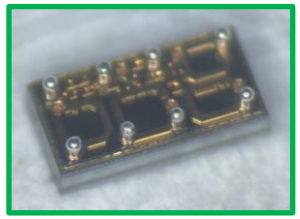
IPD 3.0

- Hybrid IPD+Acoustic

TGV vs. HRSi for N77 Filter



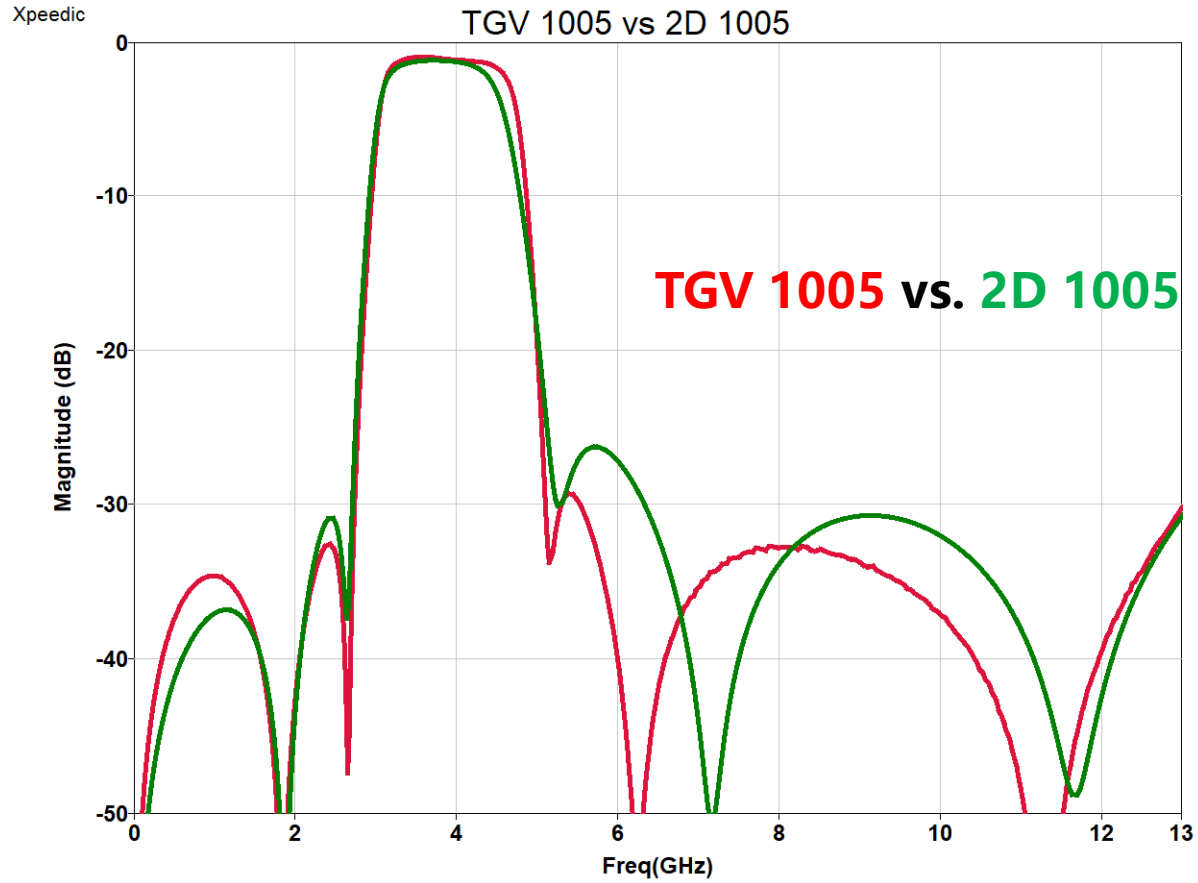
TGV 1005



HRSi 1005

20% better IL while 10% better Rejection

Item	Freq.(MHz)	IPD 1005	TGV 1005	Comparison
IL(dB)	3300~4200	1.6	1.3	↑0.3
RL(dB)	3300~4200	20	20	--
RJ. (dB)	1710~1850	42	45	↑3
	2400~2500	30	32	↑2
	2620~2690	33	35	↑2
	5150~5850	27	29	↑2
	5850~5925	30	35	↑5
	6600~8400	32	33	↑1
	9900~12600	31	35	↑4



Summary

- Wireless technology continues evolving, which poses great challenges to RFFE designs;
- Xpeedic provides a series of powerful tools to ensure first-pass RFFE designs;
- IPD provides viable solution to achieve RFFE integration and miniaturization.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